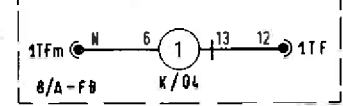


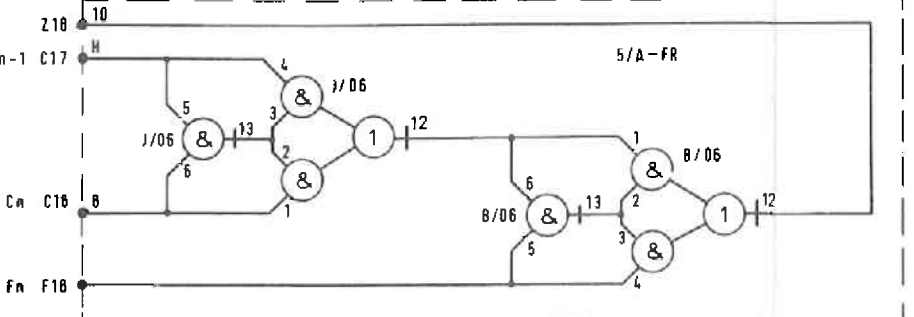
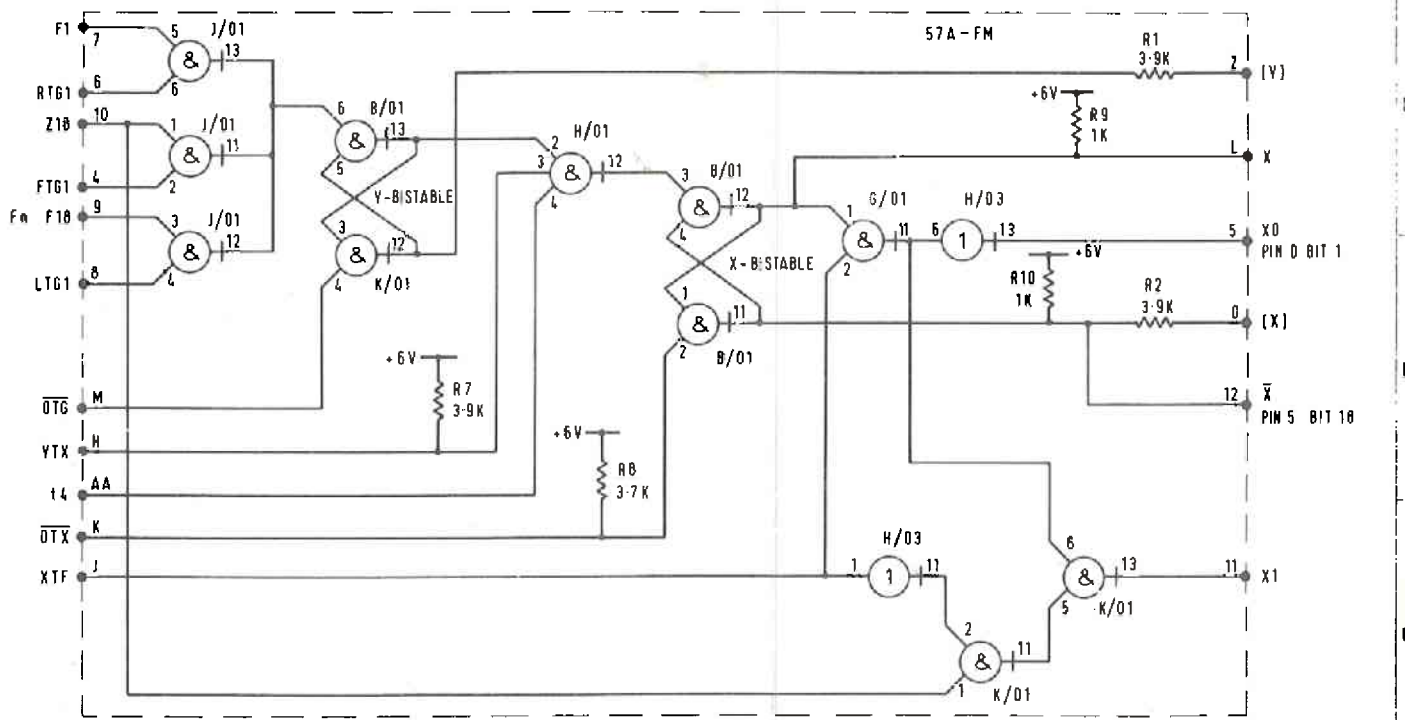
TERM	A-FE PIN	A-FJ PIN	A-FK PIN	A-FR PIN
L1	-	-	AF	AD
L2	-	AF	-	v
L3	-	-	AE	29
L4	AD	-	AD	26
RESET	-	-	AH	-

NOTE: P Reg on boards 1-13
I Reg on boards 14-17



ADDER (F UNIT)

Cn-1 C
ITF BIT 1 ONLY FROM CONTROL



The output of the Adder = $X_n - Y_n + (C_n - 1)$. Since $C_n - 1$ to Bit 1 cannot exist, the I.T.F. signal is routed to the input. Hence if I.T.F. occurs then digit 1 is added to any other input to the adder.
With bits 1-13, DTf₁ makes $Y_n = 1$. Hence if DTf₁ and VTG occur, the G register will copy the first 13 bits of the register gated into X_n . With all bits, DTf₁ and DTf₂ makes $Y_n = 1$. Hence if this occurs with FTG, a "full house" is added to X_n , ie digit 1 is subtracted.

TITLE
LOGIC OF REGISTERS
ADDING AND
OVERFLOW UNITS