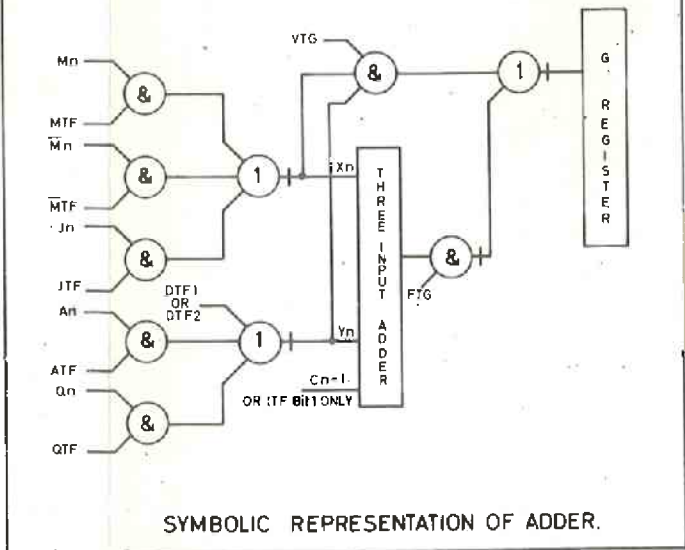


NOTE. TERMS MARKED WITH THE SUFFIX 'm' i.e. VTGm COME DIRECTLY FROM THE MATRIX AND A TRUE OUTPUT IS REPRESENTED BY 0 VOLTS.

THE OUTPUT OF THE ADDER IS EQUAL TO THE SUM OF  $X_n + Y_n + C_{n-1}$ . AS THERE CAN BE NO  $C_{n-1}$  TO BIT 1 THE ITF SIGNAL IS TAKEN TO THIS INPUT. HENCE IF ITF OCCURS THEN ONE IS ADDED TO ANY OTHER INPUT TO THE ADDER. DTF1 MAKES  $Y_n$  ON BITS 1-13 EQUAL TO 1. HENCE IF DTF1 AND VTG OCCUR, THE G REGISTER WILL COPY THE FIRST 13 BITS OF THE REGISTER GATED INTO  $X_n$ . DTF1 & DTF2 MAKES  $Y_n$  ON ALL BOARDS EQUAL TO 1. HENCE IF THIS OCCURS WITH FTG THEN A 'FULLHOUSE' IS ADDED TO  $X_n$ , I.E. ONE IS SUBTRACTED.



SYMBOLIC REPRESENTATION OF ADDER.

920B COMPUTER REGISTER MODULE AND CONTROL WAVEFORMS

TO BE READ IN CONJUNCTION WITH 322A7191