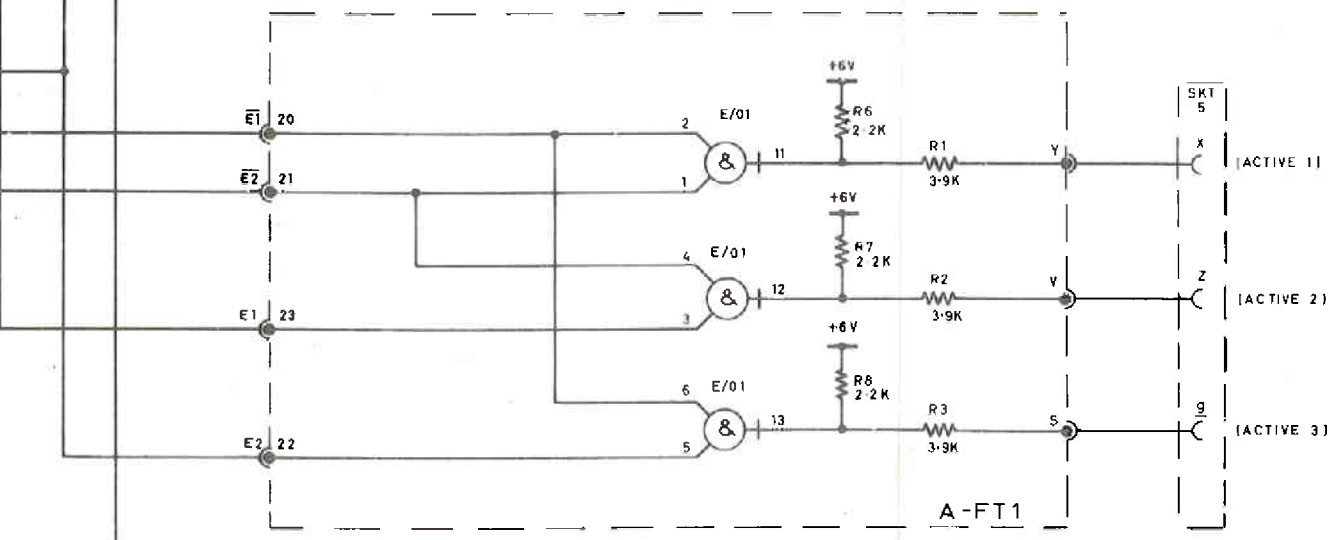


SETTING PULSES TO APPROPRIATE BITS OF THE J REGISTER



TO BE READ IN CONJUNCTION WITH 322 A 7181

920 B COMPUTER CONTROL AND INTERRUPT OVERALL LOGIC

SHT 2 OF 2

A18